Modeling of Jitter Characteristics for the Second Order Bang-Bang CDR

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ABSTRACT

Bang-Bang clock and data recovery (BBCDR) circuits are hard nonlinear systems due to the nonlinearity introduced by the binary phase detector (BPD). The specification of the CDR frequency response is determined by jitter tolerance and jitter transfer. In this paper, jitter transfer and jitter tolerance of the second-order BBCDR are characterized by formulating the time domain waveforms. As a result, a new equation is presented to obtain corner frequency. Also, the jitter tolerance is expressed in closed form as a function of loop parameters. The proposed method is general enough to be used for designing BBCDR. The analysis is verified using behavioral simulations in MATLAB. Simulation results demonstrate the validity of the result obtained by analytical equations.

KEYWORDS

Clock and Data Recovery (CDR), Bang-Bang Phase Detector (BPD), Jitter Transfer and Jitter Tolerance

1. INTRODUCTION

Nowadays, the volume of the data transported in telecommunication systems is noticeably growing, which means that the bandwidth required for data transmission is also increasing. Therefore, because of having high bandwidth, optical fiber is used for data transmission. However, after passing through the fiber, the data are distorted and their amplitude is decreased due to their non-ideal effects. Thus, the data transported by the fiber are required to be regenerated in the receiver. However, due to high transmission speed of the data, those circuits are needed which can properly act at high speed (frequency). Clock and data recovery (CDR) circuit using bang-bang (binary) phase detector (BPD) are widely used in communication systems mainly because of their high-frequency capabilities [1]. Examples include multi-gigahertz clock multipliers [2] and optical receivers (STM, SONET) [3].

The advantage of BPD over linear phase detectors is that BPD exhibits a very high gain in the vicinity of $\Delta\varphi=0$ and is able to operate at higher speeds [4]. Since, in linear detectors and in case if phase difference exists, a pulse proportional to the phase difference is generated; however, if frequency is high, the width of the produced pulse would be very narrow. In other words, the average output value of the PD would be very small and, as a result, the voltage required for adjusting frequency would not be provided and CDR would not properly work. But, if there is large or small phase difference, due to having very high gain BPD produces constant and large voltages in the output to move the CDR loop toward the lock. In other words, the BPD output has two distinct and deterministic levels depending on the sign of the input phase-difference. This has led to its application at a higher speed (frequency). The transfer characteristic of a BPD is shown in Fig.1. The output of BPD is +1 and -1 for positive and negative phase errors, respectively. Thus, CDR based on BPD (BBCDR) is a nonlinear system due to the inherent nonlinear phase to voltage transfer function of the BPD. Thus, unlike a linear CDR, the analysis of a bang–bang loop is complicated.

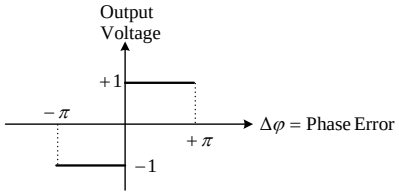

Fig.1:Transfer characteristic of the BPD.

As it is well known, the jitter at the input leads to bit errors at the output of CDR; therefore, jitter analysis is very important for evaluating the performance of BBCDR. In practical digital communication standards, the specification of the CDR frequency response is determined by jitter tolerance and transfer. The frequency

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domain characteristic of jitter transfer must meet some requirements. First, the BBCDR loop bandwidth should be very small. Second, the peak of the jitter transfer must not be greater than a specific value. The amount of peaking in the jitter transfer must be less than 0.1 dB for the SONET standard. Therefore, the analysis of peaking is required. Moreover, the jitter tolerance specifies the amount of tolerable input jitter without increasing the bit error rate at a given jitter frequency.

Many efforts have been made to analyze the nonlinear loop dynamic of BBCDR [5]-[11]. The effect of jitter can be accurately analyzed using Markov models, but their applicability is limited to first-order loop (without loop filter capacitor) [5]–[7]. In [8], the steady-state analysis of BBCDR is performed for the cases that there is not any jitter in input and the value of output jitter amplitude is derived. Moreover, [9] and [10] mainly focus on the characterization of the jitter transfer and tolerance of BBCDR in response to large sinusoidal input jitters. In [9], the jitter transfer properties are investigated for first order BBCDR (without loop capacitor) and in [10], using an approximation, a linear model of a second-order bang–bang loop is introduced and the slewing effect is utilized to derive expressions for jitter transfer, jitter tolerance and jitter generation. However, in [10] the analysis method is based on a large off-chip value assumption for the capacitor [11]. The off-chip capacitor increases the number of external components and pin count; also it couples noise from off-chip to the control voltage of the voltage-controlled oscillator (VCO) in the CDR block. Another issue is that the bond wire inductor drastically increases the high-frequency impedance of the loop filter and makes the CDR more sensitive to high-frequency noise [11]. Thus, designers are still looking for the ways for designing loop parameters and estimate the frequency response characteristic. Therefore, the first step is accurate analysis of the CDR loop.

In this paper, jitter transfer and jitter tolerance for BBCDR with a first order loop filter are characterized by formulating the time domain waveforms. As a result, new closed form equations are presented for the jitter transfer and the jitter tolerance. The proposed method is general enough to be used for designing BBCDR. The proposed analysis does not further need any assumptions on system parameters especially loop capacitance. Behavioral simulations will be used to validate the analytical results with particular emphasis on the jitter transfer and the jitter tolerance characteristics. This paper is organized as follows. Section 2 briefly reviews the BBCDR architectures in the literature. Sections 3 and 4 introduce the analysis of time domain waveforms to derive the jitter transfer and the jitter tolerance specifications, respectively. The accuracy of the proposed analysis is evaluated in section 5. Finally, the paper will be concluded in section 6.

2. BANG-BANG CDR ARCHITECTURE

Fig. 2 shows a block diagram of a typical second order BBCDR which is composed of a data sampler PD, a charge-pump, a first order loop filter and a voltage-controlled oscillator (VCO). The PD detects the phase difference between the data-sampling clock and the center of the incoming data and generates late or early signals for the charge-pump. The charge-pump supplies the loop filter that includes R_p, C_p according to the signals generated by PD. The voltage over the loop filter is the VCO control voltage and determines the frequency and phase of the sampling clock. With this feedback mechanism, the data-sampling clock tracks the center of the incoming data bits, and the clock to which the data is synchronized will be recovered in the receiver.

In some practical systems, a second capacitor is usually added in parallel with R_p and C_p and it increases the loop filter order to two. This capacitor is used to suppress the sudden jump on the VCO control voltage produced by charge injection and clock feed through of the two switches and improves the transient characteristics. If this capacitor is much smaller than C_p, for example about one-fifth to one-tenth of C_p, the time domain waveforms and frequency response remain relatively unchanged and are similar to those of the first order loop filter [13]. As a result, in this paper the added capacitor (C2) is chosen much smaller than C_p and BBCDR with a first order loop filter is analyzed. The phase-domain model of BBCDR is shown in Fig. 3. This model was implemented for a behavioral simulation to verify the accuracy of the derived equations. In Fig. 3, K_{VCO} is the VCO gain and I_p is the charge pump current.

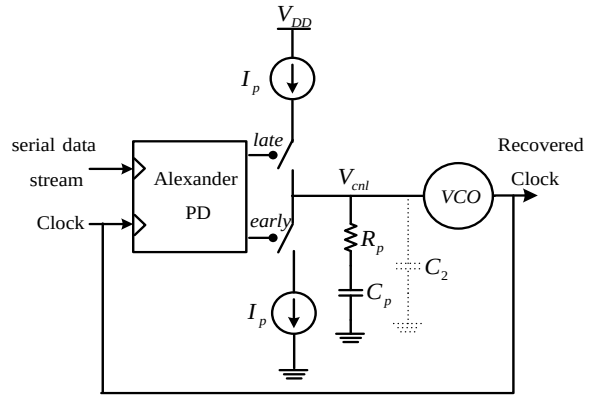


Fig.2: Structure of the second order CDR with a bang-bang phase detector.

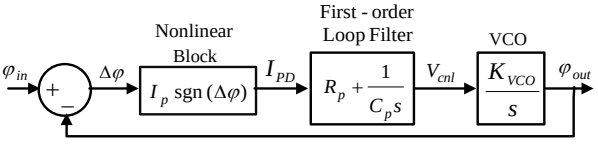


Fig.3: Phase domain model of the second order BBCDR.

3. JITTER TRANSFER ANALYSIS

The jitter transfer function is defined as the ratio of the output signal jitter to the jitter applied on the input versus frequency. Jitter transfer can be considered as a gain by which the CDR attenuates or amplifies the input jitter. Jitter transfer must meet some specifications. As an example, in SONET OC-48, the cutoff frequency, f_C, is 2MHz and the peaking is 0.1 dB [13]. In binary CDR, the jitter transfer function strongly depends on the input jitter magnitude. Thus, the linear models cannot be applied to the binary CDR analysis.

For negligible jitter peaking and jitter frequency close to f_C, the waveforms of BBCDR have typical prototypes shown in Fig. 4. Also, as the input jitter frequency exceeds f_C, the output jitter magnitude begins to fall as shown in Fig. 5. It can be reasonably assumed that all of the waveforms are symmetric around the origin and have the same period of T_P. Where, T_P is the period of the applied input sinusoidal jitter. According to appendix A, the output phase at $0 \le t \le T_P/2$ is obtained as follows

$$\varphi_{out}(t) = at^2 + bt - \frac{1}{2}aT_p t - b\frac{T_p}{4} \tag{1}$$

where,

$$a = -0.5K_{VCO}I_p / C_p \tag{2}$$

$$b = -K_{VCO}R_p I_p \tag{3}$$

The initial phase of $\varphi_{out}(t)$ occurs at t=0, which is obtained from (1) as follows [9]

$$\varphi_0 = -b\frac{T_p}{4} = \frac{K_{VCO}R_p I_p T_p}{4} \tag{4}$$

It can be seen from (1) that $\varphi_{out}(t)$ has a parabolic shape. As shown in Fig.4, the input is a sinusoidal waveform and it is reasonable to assume that $\varphi_{in}(t) = \varphi_{i,p}\sin(\omega_P t + \theta_0)$. Thus, from Fig. 4, $\sin\theta_0 = \varphi_0/\varphi_{i,p}$. Also, note that if the jitter peaking of the jitter transfer function is approximately zero, at jitter frequencies close to f_C, $\varphi_{out}(t)$ still tracks $\varphi_{in}(t)$ closely so as $\Delta\varphi$ is minimized and the jitter transfer approaches unity. In other words, $\varphi_{in}(t) \approx \varphi_{out}(t)$, for $f_p \approx f_C$. It follows that

$$\begin{aligned}\varphi_{out}(t) &= at^2 + bt - \frac{1}{2}aT_p t - b\frac{T_p}{4} \\ &\approx \varphi_{i,p}\sin(\omega_p t + \theta_0)\end{aligned} \tag{5}$$

Equation (5) holds for any t in the interval $[0, T_p/2]$ like the time mentioned in (6) that leads to an easier solution. Because of the term sin(.), considering other times in (5) makes the solution complex and finding the unknown parameter will be impossible.

$$t = T_p / 4 \tag{6}$$

Finally, the corner frequency can be derived by substituting (6) into (5) as

$$-a(\frac{T_p}{4})^2 = \varphi_{i,p}\cos\theta_0 = \varphi_{i,p}\sqrt{1 - \frac{\varphi_0^2}{\varphi_{i,p}^2}} \tag{7}$$

Replacing (4) into (7) yields

$$-a(\frac{T_p}{4})^2 = \sqrt{\varphi_{i,p}^2 - b^2(\frac{T_p}{4})^2} \tag{8}$$

And finally the equation for the corner frequency is as (9).

$$a^2(\frac{T_p}{4})^4 + b^2(\frac{T_p}{4})^2 = \varphi_{i,p}^2 \tag{9}$$

Equation (9) can be used to derive an approximate value for corner frequency ($f_C = 1/T_P$) of the jitter transfer. It is therefore possible to approximate the entire jitter transfer with a first order low pass filter as (10)

$$\frac{\varphi_{out}}{\varphi_{in}}(s) = \frac{1}{1 + \frac{s}{\omega_C}} \tag{10}$$

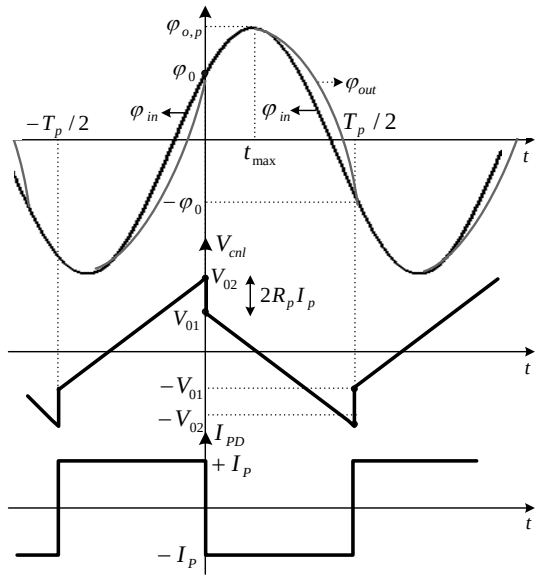


Fig.4: Waveforms of the BBCDR at jitter frequency close to fC.

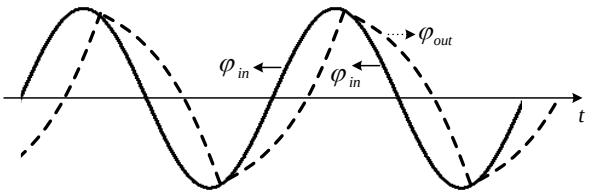


Fig.5: Waveforms of the BBCDR as jitter frequency exceeds fC.

As expected, it can be seen from (9) that in binary CDR, the bandwidth of the jitter transfer depends on the input jitter magnitude ($\varphi_{i,p}$). Also, to increase f_C, one of loop parameters, R_p or I_p or K_{VCO} must be raised. But as C_p increases, the jitter bandwidth is decreased. Note that, the above analysis is valid when the value of the jitter peaking is approximately zero. This is equivalent to a large damping factor in the vicinity of ω_C [10]. Thus, this condition should be met. The jitter peaking does not occur when the maximum output phase stays smaller than the maximum input phase. In order words, the expression (11) should be hold.

$$\varphi_{o,p} \le \varphi_{i,p} \tag{11}$$

As shown in appendix B, the following important result can be derived as (12).

$$-\frac{b^2}{4a} = \frac{1}{2} K_{VCO} R_p^2 I_p C_p \le \frac{2}{3}\varphi_{i,p} \tag{12}$$

Equation (12) is a sufficient condition to guarantee the jitter peaking is negligible. If R_p, I_p and K_{VCO} are held constant and C_p is decreased, the stability would be definitely destroyed. However, K_{vco} is the VCO parameter and cannot be adjusted by the designer. Thus, if the capacitor is selected to be small, other parameters can be increased so that the stability is not destroyed. The capacitor cannot be selected very small since irrational values would be resulted for I_p and R_p. However, if the product of $R_pC_pI_p$ is excessively increased, the condition (12) is violated and peaking would definitely occur in the output. Thus, the CDR parameters should be designed so that the product of $R_pI_pC_p$ is at the maximum to maximize stability. Additionally, condition (12) should not be violated in order not to have any peaking in the output. Therefore, designing should be in the boundary state of (12). Investigating end times of intervals, from (12) the unknown parameter b can be expressed as

$$b^2 = -\frac{8}{3} a \varphi_{i,p} > 0 \tag{13}$$

Combining (13) and (9) gives (14).

$$a^2 \left(\frac{T_p}{4}\right)^4 - \frac{8}{3} a \varphi_{i,p} \left(\frac{T_p}{4}\right)^2 = \varphi_{i,p}^2 \tag{14}$$

In the SONET standard, $T_P = 1/f_C$ is given. Also, $\varphi_{i,p}$ is known. Thus, the negative value of the unknown parameter 'a' is derived by solving (14). As a result, (14) is generally used for designing the BBCDR loop parameters to meet SONET jitter transfer requirements (loop bandwidth and jitter peaking). The design methodology for the CDR is described as follows

1) The parameters $T_P = 1/f_C$ and input jitter amplitude ($\varphi_{i,p}$) are given. Therefore, using (14), the negative value of the parameter *a* is calculated.

2) Having the VCO gain and the on-chip loop capacitor (C_p) the charge pump current I_p can be easily obtained from (2).

3) In order to minimize jitter peaking, (12) must be satisfied. Thus, the negative value of b can be determined and the loop resistor can be calculated using (3).

4. JITTER TOLERANCE ANALYSIS

In the CDR, since the incoming data may exhibit substantial noise and experience considerable attenuation, the data bits must ideally be sampled by the recovered clock at their midpoints so as provide maximum distance from the decision threshold and data transition points. This concept has been shown in Fig. 6. For slowly varying jitter at the incoming data, the recovered clock tracks the phase variations in order to accurately sampling the data to avoid increasing the BER. For rapidly varying jitter, the clock can not fully track the input phase variations, failing to sample the data optimally and creating a greater BER. The jitter tolerance determines the peak-to-peak amplitude of the input jitter for a given jitter frequency, that can be applied to the CDR input without worsening the bit error rate (BER) of 10^{-12}. Jitter tolerance represents the ability of CDR to recover an incoming serial data correctly despite the applied jitter. As illustrated in Fig. 7, the specification is typically described by a jitter tolerance mask as a function of the jitter frequency. As an example, in SONET OC-48, the CDR must withstand a peak-to-peak jitter of 15 UI [UI=Unit Interval] if the jitter frequency varies at a rate below 100Hz [12].

In order to achieve a good jitter tolerance, a high bandwidth is required so that CDR can track the jittery input signal and be able to recover the incoming serial data. On the contrary, jitter transfer compliance is achieved by limiting the bandwidth of CDR to ensure that a higher frequency jitter is reduced. However, in binary CDR, the loop bandwidth cannot be defined in a given value because the loop bandwidth strongly varies with the input jitter magnitude.

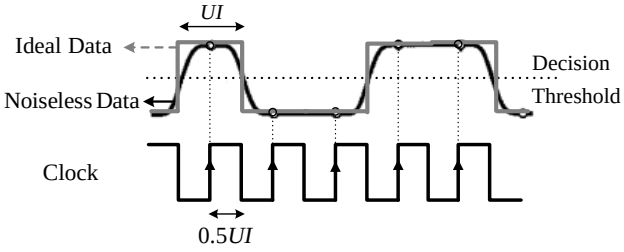


Fig.6: Noiseless data sampled by clock.

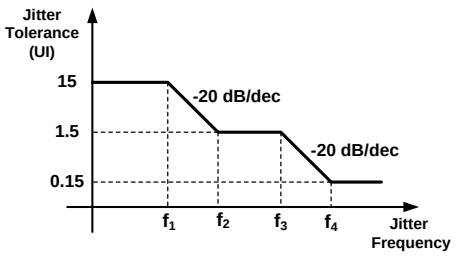


Fig.7: Jitter Tolerance Mask.

As input jitter frequency exceeds the loop bandwidth frequency, the output jitter magnitude begins to fall as shown in Fig. 8. Similar to the analysis of section 3, the output phase at $0 \le t \le T_P/2$ can be obtained from (1). As shown in Fig.8, the input signal is a sinusoidal waveform and can be expressed as follows

$$\varphi_{in}(t) = -\varphi_{i,p} \sin(\omega_p t - \theta_0) \tag{15}$$

where, $\sin\theta_0 = \varphi_0/\varphi_{i,p}$.

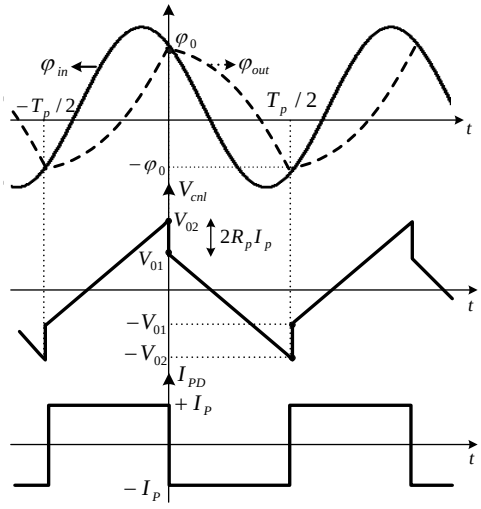


Fig.8: Waveforms of the BBCDR as jitter frequency exceeds fC.

It is instructive to quantify the jitter tolerance of a typical CDR loop and compare the result with the mask shown in Fig. 6. At a given jitter frequency, we must increase the magnitude of the input excess phase, $\varphi_{in}(t)$, until the bit error rate begins to rise. In other words, the phase error, $\Delta\varphi$, approaches π [= half unit interval (UI)], bringing the sampling edge of the clock close to the zero-crossing points of data. Thus, as shown in Fig. 6, an approximate condition to avoid increasing BER is as follows [10]:

$$|\Delta\varphi|_{\max} = |\varphi_{in}(t) - \varphi_{out}(t)|_{\max} \le \frac{1}{2}UI = \pi \tag{16}$$

Equivalently, form (1) and (15) we have:

$$\Delta\varphi = \varphi_{in}(t) - \varphi_{out}(t)$$
$$\approx -\varphi_{i,p}\sin(\omega_p t - \theta_0) - at^2 - bt + \frac{1}{2}aT_p t + b\frac{T_p}{4} \tag{17}$$

The time at which $\Delta\varphi_{max}$ occurs can be calculated by equating the first derivate of (17) to zero. As can be seen, the calculation of this time is difficult. To resolve this problem, we approximate $\varphi_{out}(t)$ by (18). This approximation is shown in Fig. 9 and can be explained in the following. The time when $\Delta\varphi_{max}$ occurs is approximately equal to the time at which $\Delta\varphi_{app}|_{max} = \varphi_{in} - \varphi_{out}|_{app}$ reaches the maximum value.

$$\varphi_{out}(t)|_{app} \approx \varphi_0\cos(\omega_p t) \tag{18}$$

where, φ_0 can be obtained according to Fig. 8 and by (15) for t=0 as

$$\varphi_0 = \varphi_{i,p}\sin\theta_0 \tag{19}$$

Therefore, from (15), (18) and (19) we get

$$\Delta\varphi_{app}|_{\max} = \varphi_{in} - \varphi_{out}|_{app} = -\varphi_{i,p}\sin\omega_p t.\cos\theta_0 \tag{20}$$

As a result, the time when $\Delta\varphi_{app}|_{max} = \varphi_{in} - \varphi_{out}|_{app}$ is maximized, can easily be calculated. Equation (20) reveals that $\Delta\varphi_{app}|_{max}$ occurs at $\omega_p t = \pi/2$ or, equivalently, $t = T_p/4$. Coming back to (17) and substituting $t = T_p/4$, the maximum phase error is calculated as

$$|\Delta\varphi|_{\max} = -a(\frac{T_p}{4})^2 + \varphi_{i,p}\cos\theta_0$$
$$= -a(\frac{T_p}{4})^2 + \varphi_{i,p}\sqrt{1 - \frac{\varphi_0^2}{\varphi_{i,p}^2}} \tag{21}$$

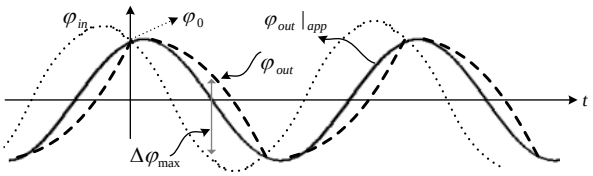


Fig.9: Approximation of φout(t) (dashed lines) by (18) (solid lines).

Replacing (4) into (21), yields

$$|\Delta\varphi|_{\max} = -a(\frac{T_p}{4})^2 + \sqrt{\varphi_{i,p}^2 - b^2(\frac{T_p}{4})^2} \tag{22}$$

where, $T_p = 2\pi/\omega_p$. Equating $\Delta\varphi_{max}$ to π yields the maximum tolerable input jitter $\varphi_{i,p} = G_{JT}$:

$$G_{JT} = \varphi_{i,p} = \frac{\pi}{\omega_p^2}\sqrt{\omega_p^4 + (\frac{2a\pi + b^2}{4})\omega_p^2 + (\frac{a\pi}{4})^2} \tag{23}$$

The above equation contains two poles at the origin and two zeros. Consequently, as depicted in Fig. 10, $|G_{JT}|$ fall at a rate of 40 dB/dec for $\omega_p < \omega_{p1}$ and at 20 dB/dec for $\omega_{p1} < \omega_p < \omega_{p2}$, approaching 1/2 UI [=π] for $\omega_p > \omega_{p2}$. The SONET mask is also given in this plot.

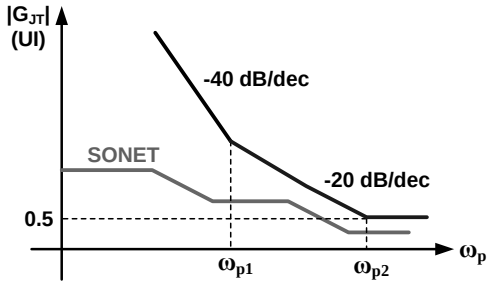


Fig.10: Jitter Tolerance Mask.

The corner frequencies can be calculated by the following relationship. Equation (23) indicates that the jitter tolerance is proportional to the VCO gain, CP current and filter resistor while inversely proportional to the smaller capacitor in the filter. Using (23) at a given input jitter amplitude, $\varphi_{i,p}$, the frequency at which $\Delta\varphi_{max}$ will be equal to π is obtained by solving the following equation.

$$(1 - \frac{\varphi_{i,p}^2}{\pi^2})\omega_p^4 + (\frac{2a\pi + b^2}{4})\omega_p^2 + (\frac{a\pi}{4})^2 = 0 \tag{24}$$

A comparison of the presented analysis with simulation results will be demonstrated in Section 5.

5. SIMULATION RESULTS AND DISCUSSION

In order to validate the proposed analysis and

modeling approach, two design examples are carefully performed and simulated using MATLAB simulator. System level simulation is performed by the phase-domain model of BBCDR which has been shown in Fig. 3. The corresponding loop parameters are calculated using the design methodology described in Section 3. In these system level simulations, CDRs are designed for π input jitter amplitude although the loop parameters vary from design to design. As an example, the designing method according to the SONET-OC-48 standard was given, in which f_C=2MHz. Thus

$$f_C = 2MHz \quad \Rightarrow \quad \frac{T_p}{4} = \frac{1}{4f_C} = 0.125\times10^{-6}$$

By substituting this value of Tp/4 in (14) and by assuming $\varphi_{i,p}=\pi$, the following can be obtained

$$a = 6.03\times10^{14} \quad , \quad a = -6.7\times10^{13}$$

Considering what was mentioned previously, the value of $a=-6.7\times10^{13}<0$ is acceptable. In such a case, (13) is used in order to have less peaking:

$$b^2 = -\frac{8}{3}a\varphi_{i,p} = 5.6\times10^{14} \quad \Rightarrow \quad b = \pm23.7\times10^{6}$$

Since the value of *b* is negative, thus $b=-23.7\times10^6$. The value of K_{VCO} is usually definite and is selected equal to 0.2×10^9 Hz/V. Moreover, value of C_p capacitor is on-chip and is selected equal to 100pf. Therefore, R_p and I_p should be calculated. The values of *a* and *b* result in

$$a = -\frac{1}{2}K_{VCO}\frac{I_p}{C_p} = -\frac{1}{2}\times0.2\times10^9\times\frac{I_p}{100\times10^{-12}} = -6.7\times10^{13}$$

$$\Rightarrow \quad I_p \approx 70\mu A$$

and

$$b = -K_{VCO}R_pI_p = -0.2\times10^9\times R_p\times70\times10^{-6} = -23.7\times10^6$$

$$\Rightarrow \quad R_p \approx 1.8K\Omega$$

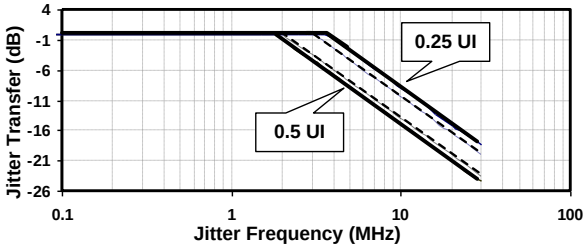
Equations *a* and *b* demonstrate that, with the increase in the value of capacitor, I_p and R_p increases and decreases, respectively. The capacitor cannot be selected very small since irrational values would be resulted for I_p and R_p. Table 1 shows the parameter values of the designed CDRs. In order to validate the analysis, the values designed for loop parameters are the reasonable values for practical implementation as well which has been confirmed in [9] and [13]. As it can be seen from (9) and (12), in OC-192 the CDR bandwidth is very small and creates a small I_p and a large resistor from (2) and (3). Thus, the loop capacitor is increased and K_{VCO} is reduced to obtain reasonable values of I_p and R_P.

TABLE 1
CDRS LOOP PARAMETERS

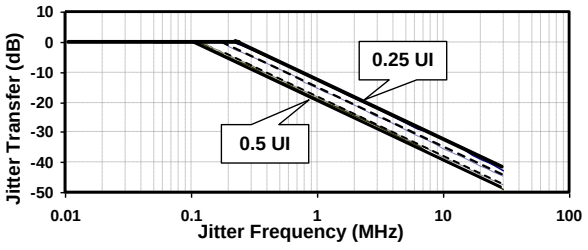
SONET	OC-48	OC-192
f_C	2 MHz	120 KHz
C_p	100 pf	500 pf
C_2=0.05C_p	5 pf	25 pf
K_{VCO}	200MHz/V	50MHz/V
I_p	70μA	100μA
R_P	1.8KΩ	5.7KΩ

A. Jitter Transfer Simulations

System level simulation is performed by the phase-domain model of the BBCDR which has been shown in Fig. 3. In order to achieve the jitter transfer characteristic through simulation, sinusoidal jitter with varying amplitude was applied at frequencies from 50 kHz to 30 MHz and at each jitter frequency, the output jitter amplitude is measured. For example, the jitter with an amplitude of 0.5UI and a frequency of 5MHz is applied as $\varphi_{in}=\pi\sin(2\pi\times5\times10^6t)$. Then, the magnitude of $\varphi_{out}(t)$ is measured which equals $\varphi_{o,p}$=1.14rad. After that, the $\varphi_{o,p}/\varphi_{i,p}$ ratio is expressed in dB, that is $20\log(1.14/\pi)$= -8.8 dB. The output amplitude is also measured for other input frequencies in the same method and the $\varphi_{o,p}/\varphi_{i,p}$ ratio is expressed in dB. Jitter transfer characteristic is obtained through connecting these points. Fig.11 plots the theoretical and simulated jitter transfer of both designed CDRs. This plot reveals a -20dB/dec roll-off in terms of jitter frequency. A comparison between simulated and calculated values shows the accuracy of analytical equations. As predicted by the analysis and according to Fig. 11, the corner frequency of the jitter transfer curve is decreased by increasing the input jitter magnitude. Thus, if $\varphi_{i,p}$ varies, ω_p is obtained from (14). The corner frequency values for different input jitter amplitudes are summarized in Table 2. Also, Table 3 shows the jitter peaking values for different input jitter amplitudes for the two designed examples. As predicted, the jitter peaking is less than 0.1dB.



(a)



(b)

Fig.11: Simulated (solid lines) and calculated (dashed lines) jitter transfer of (a) SONET OC-48 and (b) SONET OC-192 for different input jitter amplitudes.

TABLE 2
THE CORNER FREQUENCY FOR DIFFERENT INPUT JITTER AMPLITUDES

$\varphi_{i,p}$ (UI)	f_C			
	OC-48		OC-192	
	calculated	simulated	calculated	simulated
0.5	2MHz	1.97MHz	120KHz	120KHz
0.25	2.9MHz	3 MHz	175KHz	180KHz

TABLE 3
THE JITTER PEAKING FOR DIFFERENT INPUT JITTER AMPLITUDES

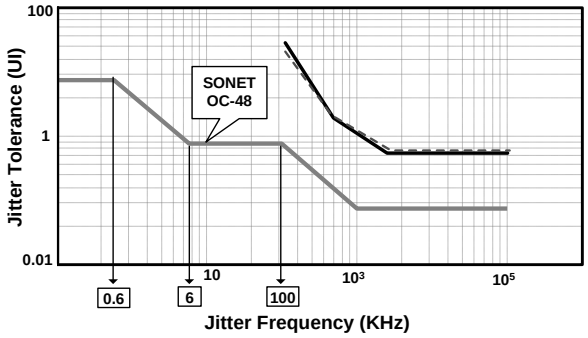
$\varphi_{i,p}$ (UI)	Jitter Peaking (dB)	
	OC-48	OC-192
	simulated	simulated
0.5	0.03	0.02
0.25	0.055	0.04

B. Jitter Tolerance Simulation

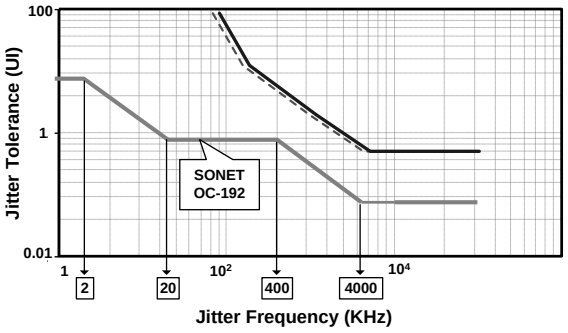
Jitter tolerance is a measure of the CDR capability in tolerating the input jitter and it is usually achieved by applying a sinusoidal jitter with different amplitudes at a given frequency range. Thus, at a given jitter frequency, we must increase the amplitude of the input jitter, $\varphi_{in}(t)$, and observe $\Delta\varphi = \varphi_{in}(t) - \varphi_{out}(t)$ until the maximum phase difference become equal to π .Therefore, the maximum jitter amplitude, as a function of jitter frequency at which the maximum phase difference is equal to π, is called jitter tolerance. For example, for OC-48 we apply $\varphi_{in}=\varphi_{i,p}\sin(2\pi\times210\times10^3 t)$ and $\varphi_{i,p}$ is gradually increased until $\Delta\varphi_{max}=\pi$. It can be seen that in $\varphi_{i,p}=12.5UI=25\pi$, $\Delta\varphi_{max}=\pi$ will take place. Therefore, the maximum tolerable input jitter amplitude for a jitter with a frequency of 210 KHz will be 12.5UI. This method is applied in different frequencies and the maximum tolerable $\varphi_{i,p}$ has been obtained for each frequency. The jitter tolerance curve is plotted by connecting these points. The simulated and calculated values of the maximum tolerable input jitter amplitudes for different jitter frequencies are summarized in Table 4. The calculated values of the jitter frequency are given by (24). Fig. 12 shows the theoretical and simulated jitter tolerance of both CDRs. As seen, the good agreement between the closed-form analytical expression (23) and the simulation results confirms the proposed analysis. As expected, $|G_{JT}|$ falls at a rate of approximately 40dB/dec at very low jitter frequencies and at 20dB/dec for greater ω_p and finally, approaching π at high ω_p. The SONET mask for OC-48 and OC-192 are also shown in Fig. 12, which shows that the SONET mask is satisfied.

TABLE 4
SUMMARY OF THE SIMULATED AND CALCULATED RESULTS

$\varphi_{i,p}$ (UI)	The frequency at which $\Delta\varphi_{max}=\pi$ (KHz)			
	OC-48		OC-192	
	calculated	simulated	calculated	simulated
15	210	190	170	150
12	235	215	195	175
8	290	275	290	280
4	415	410	580	565
1	1020	1050	2400	2380



(a)



(b)

Fig.12: Simulated (solid lines) and calculated (dashed lines) jitter transfer of (a) SONET OC-48 and (b) SONET OC-192 for different input jitter amplitudes.

6. CONCLUSION

The jitter transfer and jitter tolerance analysis of second-order bang-bang CDR has been presented and also, good analytical equations were derived. The proposed approach offers two advantages compared to the conventional designing methods. First, this approach does not consider any value restriction to the capacitor. Second, a new condition has been presented to guarantee that the value of jitter peaking is approximately zero. The accuracy of the presented expressions was verified through system level simulations. The results in this work would help designers to optimize the jitter performance of BBCDR in a system level design.

7. APPENDIX

A. The Output Phase Equation

As depicted in Fig.4, the waveform of VCO control voltage (V_{cnl}) can be written as follows

$$V_{cnl}(t)=\begin{cases}\dfrac{I_p}{C_p}t+V_{02} & -T_p/2\le t<0\\ -\dfrac{I_p}{C_p}t+V_{01} & 0\le t\le T_p/2\end{cases} \quad (25)$$

As I_{PD} jumps between $-I_P$ and $+I_P$, due to resistor the oscillator voltage control experiences a jump of $2R_PI_P$. Thus

$$V_{02}=2R_pI_p+V_{01} \quad (26)$$

From Fig. 4, since for $0\le t\le T_P/2$, the V_{cnl} reaches $-V_{02}$ at $t=T_P/2$, using (25) and (26) we can write

$$-\frac{I_p}{C_p}\frac{T_p}{2}+V_{01}=-V_{02}=-2R_pI_p-V_{01} \quad (27)$$

$$V_{01}=-R_pI_p+\frac{I_p}{C_p}\frac{T_p}{4} \quad (28)$$

Thus, the waveform of VCO control voltage (V_{cnl}) is obtained as

$$V_{cnl}(t)=\begin{cases}\dfrac{I_p}{C_p}t+R_pI_p+\dfrac{I_pT_p}{4C_p} & -T_p/2\le t<0\\ -\dfrac{I_p}{C_p}t-R_pI_p+\dfrac{I_pT_p}{4C_p} & 0\le t\le T_p/2\end{cases} \quad (29)$$

The output phase can be derived as the integration of $K_{VCO}V_{cnl}$

$$\varphi_{out}(t)=\begin{cases}K_{VCO}(\dfrac{1}{2}\dfrac{I_p}{C_p}t^2+R_pI_pt+\dfrac{I_pT_p}{4C_p}t)+\varphi_0\\ \quad , -T_p/2\le t<0\\ K_{VCO}(-\dfrac{1}{2}\dfrac{I_p}{C_p}t^2-R_pI_pt+\dfrac{I_pT_p}{4C_p}t)+\varphi_0\\ \quad , 0\le t\le T_p/2\end{cases} \quad (30)$$

$\varphi_{out}(t)$ at $0\le t\le T_P/2$ can be simplified as

$$\varphi_{out}(t)=at^2+bt-\frac{1}{2}aT_pt+\varphi_0 \quad (31)$$

where, the parameters *a* and *b* are obtained from (2) and (3), respectively. According to Fig.4, since $\varphi_{out}(0)=\varphi_0=-\varphi_{out}(T_P/2)$, using (31) we have

$$\varphi_0=-a(\frac{T_p}{2})^2-b\frac{T_p}{2}+\frac{1}{2}aT_p\frac{T_p}{2}-\varphi_0 \quad (32)$$

And,

$$\varphi_0=-b\frac{T_p}{4}=\frac{K_{VCO}R_pI_pT_p}{4} \quad (33)$$

Substituting (33) into (31), the output phase at $0\le t\le T_P/2$ can be rewritten as

$$\varphi_{out}(t)=at^2+bt-\frac{1}{2}aT_pt-b\frac{T_p}{4} \quad (34)$$

B. New Condition to Avoid Jitter Peaking

Fig. 4 reveals that the maximum point of $\varphi_{out}(t)$ occurs at $t=t_{max}$, which is obtained from (34) as (35)

$$t_{\max}=-\frac{b-\frac{1}{2}aT_p}{2a}=\frac{1}{4}T_p-\frac{b}{2a} \quad (35)$$

Substituting (35) into (34), $\varphi_{o,p}$ can be easily obtained as (36)

$$\varphi_{o,p}=-\frac{a}{16}T_p^2-\frac{b^2}{4a} \quad (36)$$

Replacing (35) into (11) we have,

$$\varphi_{o,p}=-\frac{a}{16}T_p^2-\frac{b^2}{4a}\le\varphi_{i,p} \quad (37)$$

and hence

$$-\frac{\varphi_{i,p}}{a}-\frac{b^2}{4a^2}\le(\frac{T_p}{4})^2 \quad (38)$$

Substituting (38) into (9), we have:

$$a^2(-\frac{\varphi_{i,p}}{a}-\frac{b^2}{4a^2})^2+b^2(-\frac{\varphi_{i,p}}{a}-\frac{b^2}{4a^2})\le\varphi_{i,p}^2 \quad (39)$$

Using (2) and (3), the following important result can be derived as (40).

$$-\frac{b^2}{4a}=\frac{1}{2}K_{VCO}R_p^2I_pC_p\le\frac{2}{3}\varphi_{i,p} \quad (40)$$

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